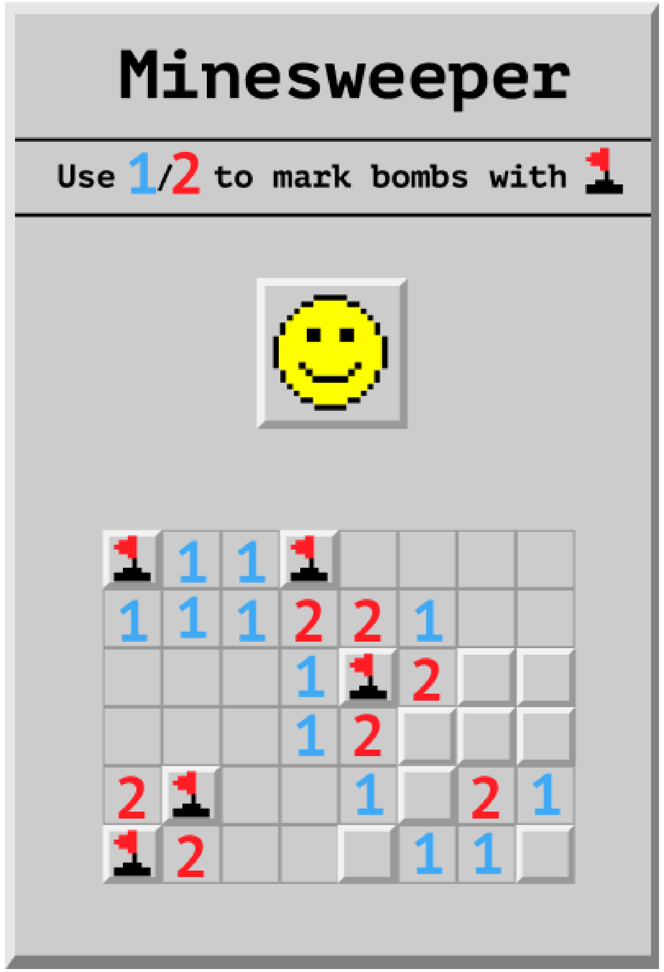
Erasure Minesweeper: exploring hybrid-erasure surface code architectures for efficient quantum error correction

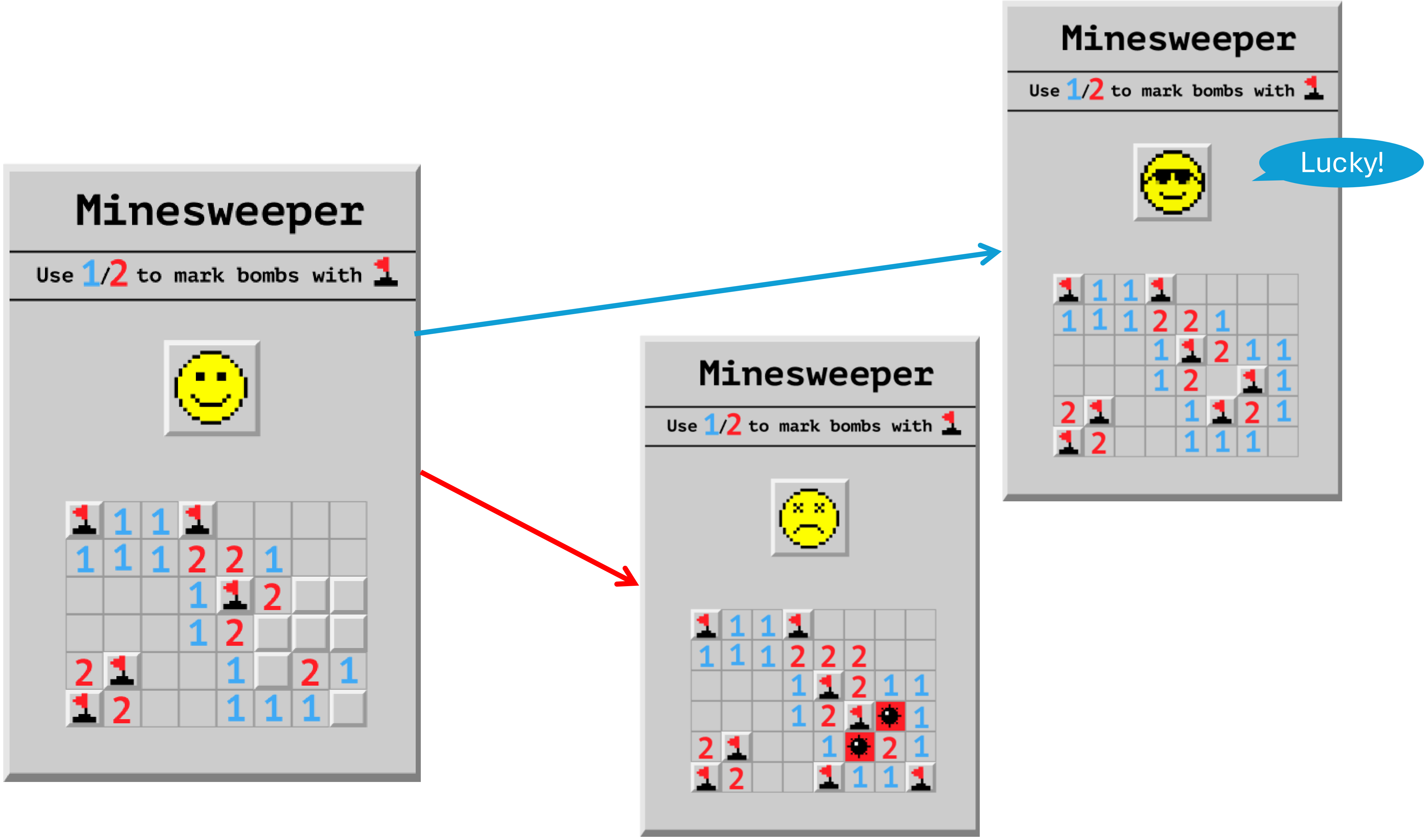
Jason D. Chadwick*, Mariesa H. Teo*, Joshua Viszlai*,
Willers Yang*, and Frederic T. Chong

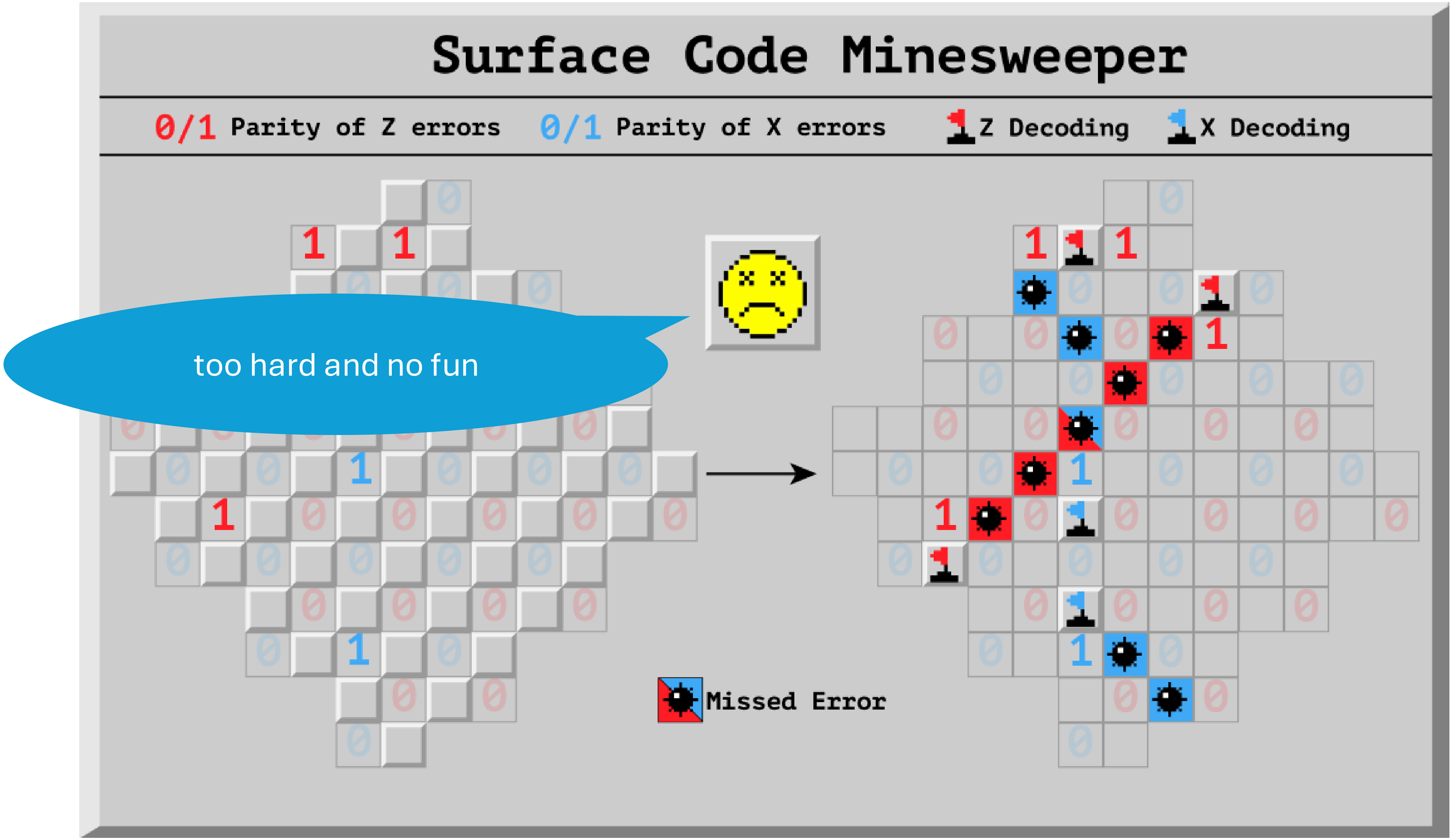
* indicates equal contribution

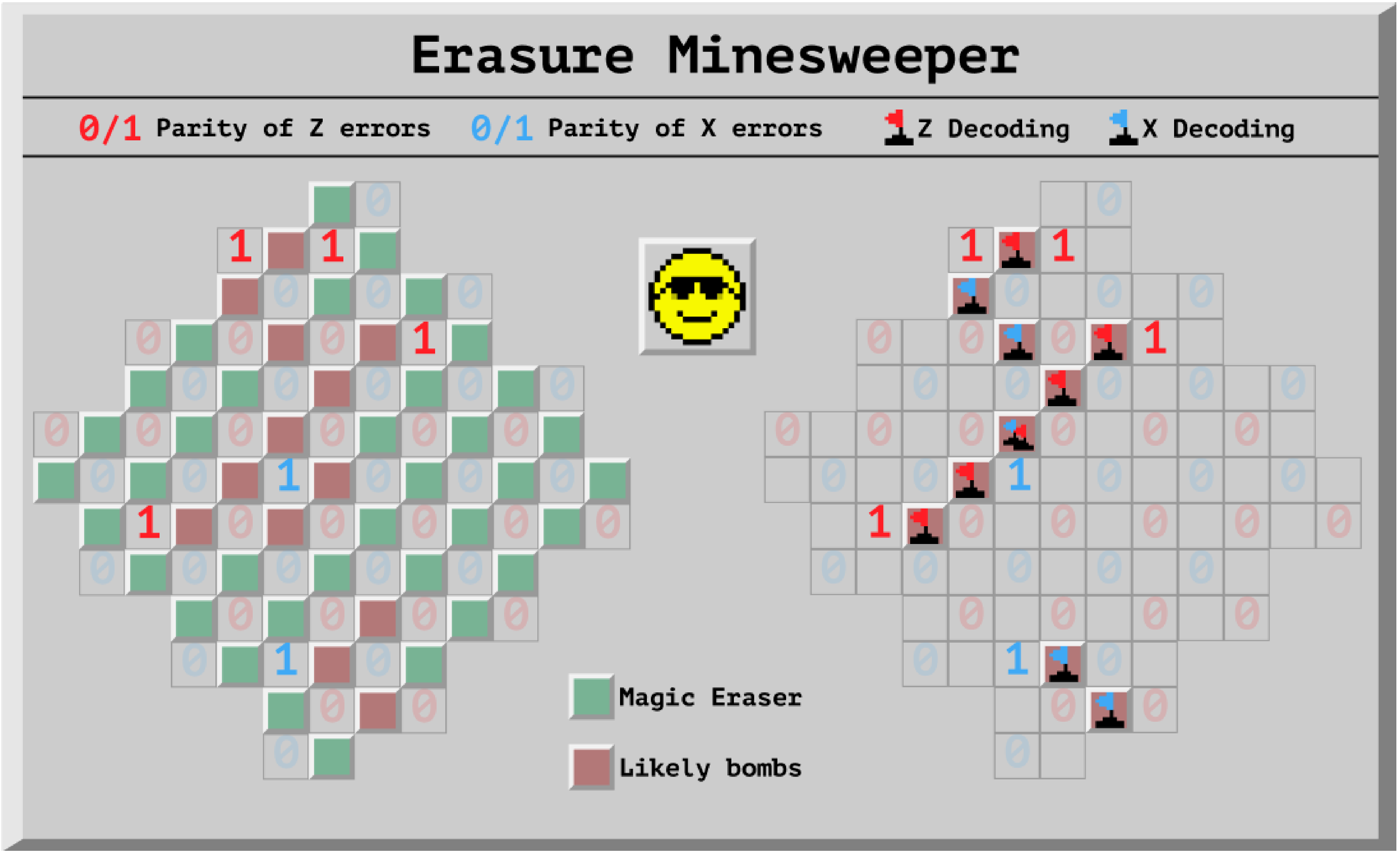
Part 1: Surface Codes as Minesweeper

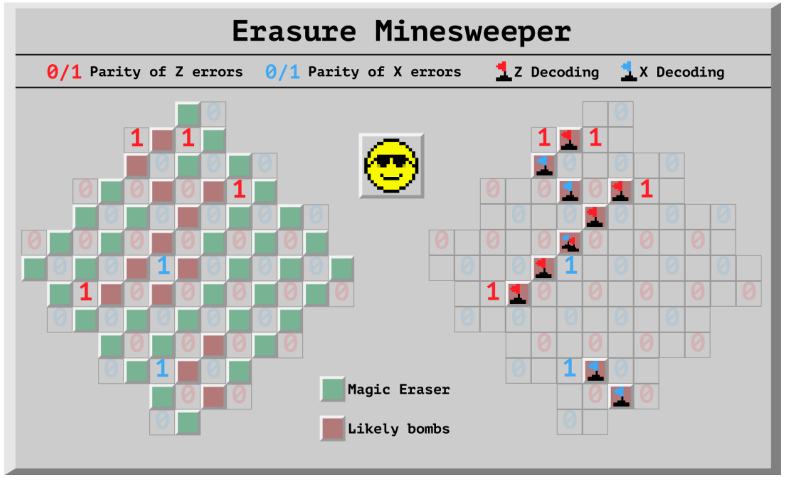
Willers Yang


Minesweeper
Use 1/2 to mark bombs with

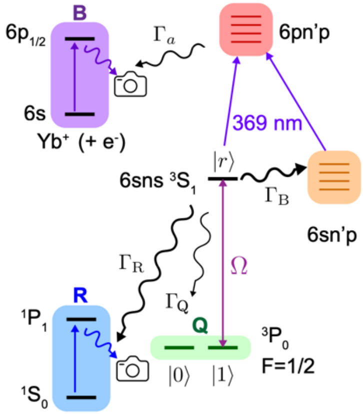

Minesweeper
Use 1/2 to mark bombs with
Minesweeper
Use 1/2 to mark bombs with
Lucky!
Minesweeper
Use 1/2 to mark bombs with

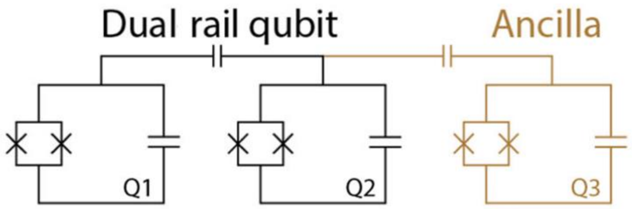

Surface Code Minesweeper
0/1 Parity of Z errors
0/1 Parity of X errors
Z Decoding
X Decoding
too hard and no fun
Missed Error


Erasure Minesweeper
0/1 Parity of Z errors
0/1 Parity of X errors
Z Decoding
X Decoding
Magic Eraser
Likely bombs



Low-overhead realizations



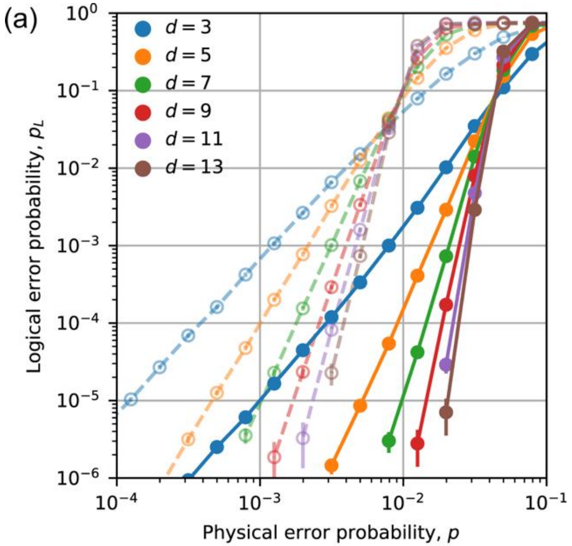


Much better error suppression

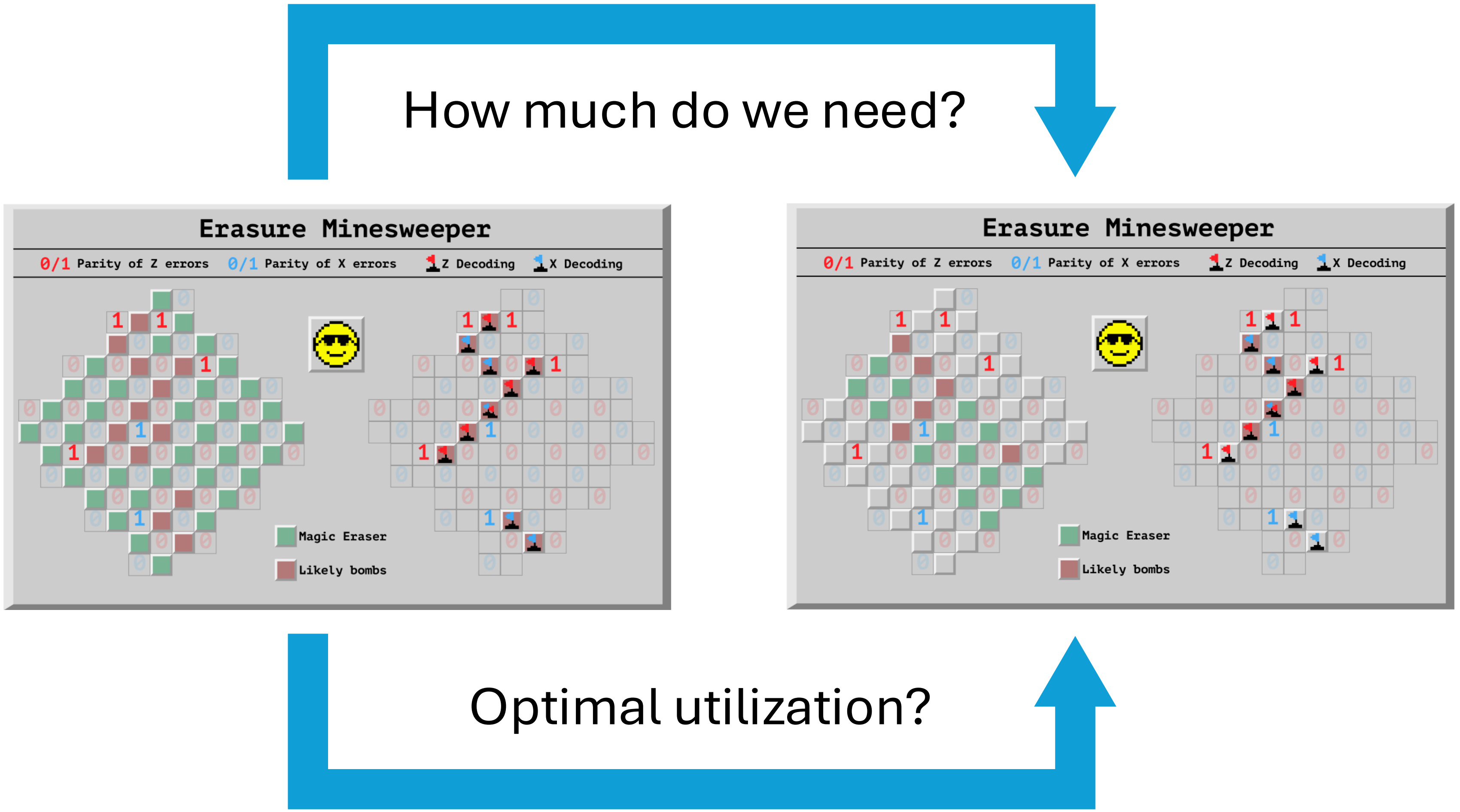
$$p \rightarrow \left(\frac{p}{p_{th}}\right)^{d_{eff}}$$

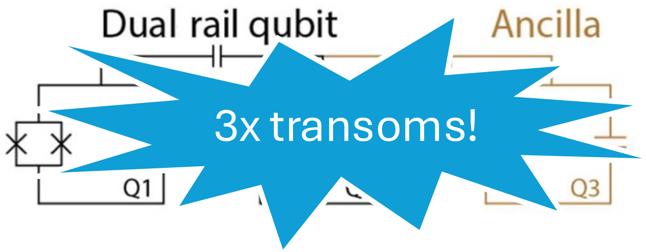
$$\left\lfloor\frac{d+1}{2}\right\rfloor \xrightarrow{\cdot\ \times 2} d$$

$$\sim 1\% \xrightarrow{\cdot\ \times 5} \sim 5\%$$



[1] Levine et al., "Demonstrating a Long-Coherence Dual-Rail Erasure Qubit Using Tunable Transmons", PRX 14, 011051 (2024)
[2] Wu, Y., Kolkowitz, S., Puri, S. *et al*. Erasure conversion for fault-tolerant quantum computing in alkaline earth Rydberg atom arrays. *Nat Commun* **13**, 4657 (2022).



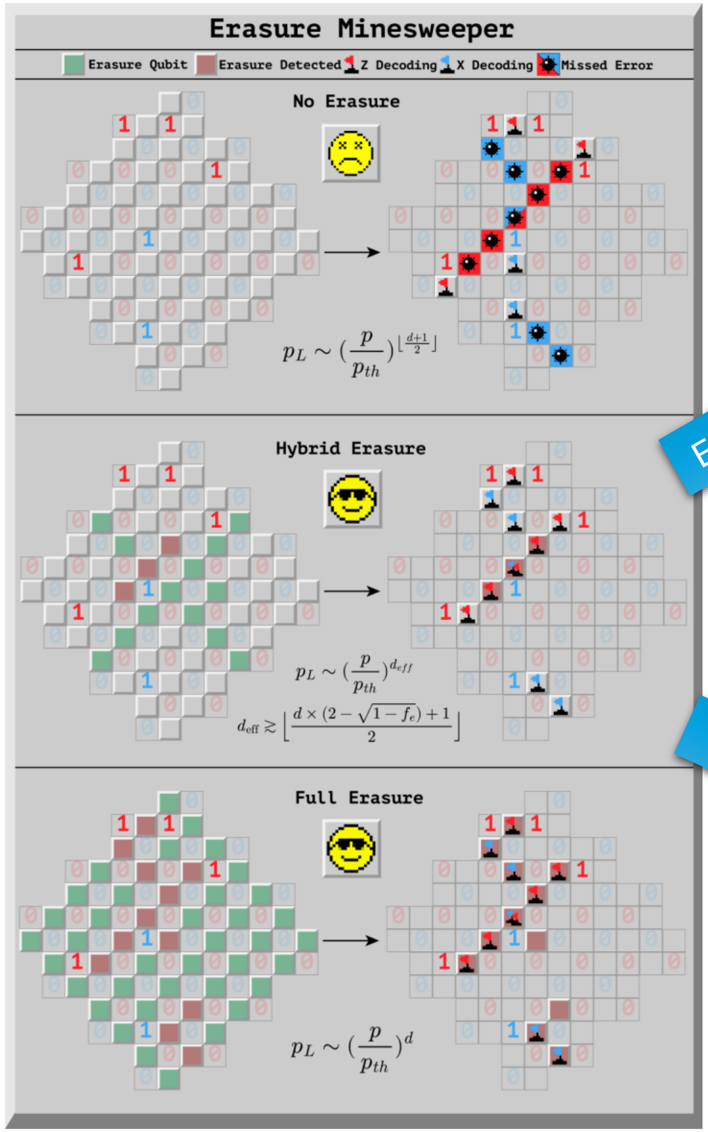


$$p \to \left(\frac{p}{p_{th}}\right)^{d_{eff}}$$

$$\left\lfloor \frac{d+1}{2} \right\rfloor \xrightarrow{\times 2} d$$

$$\sim 1\% \xrightarrow{\times 5} \sim 5\%$$

[1] Levine et al., "Demonstrating a Long-Coherence Dual-Rail Erasure Qubit Using Tunable Transmons", PRX 14, 011051 (2024)



Effective Distance

Prop: *Given a distance-d rotated surface code C. If the support of all logical operators of C contain at least k erasure qubits, the logical error rate of $C(d,k)$ is*

$$p_L \lesssim p_{phys}^{\lfloor (d+k+1)/2 \rfloor},$$

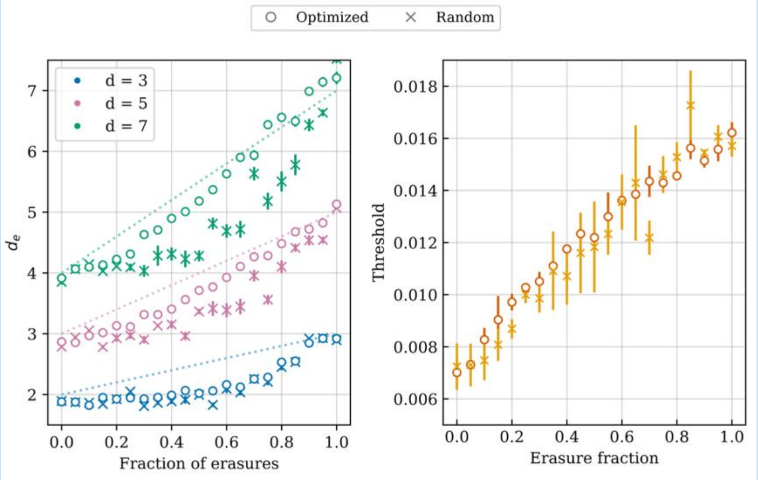
to leading order in p_{phys} under code-capacity level noise p_{phys}.

Corr: *Given hybrid-erasure surface code $C^*(f_e)$ with f_e fraction of erasures placed optimally, the effective distance is*

$$d_{eff} \geq \left\lfloor \frac{d \times (2 - \sqrt{1-f_e} + 1)}{2} \right\rfloor - \epsilon d$$

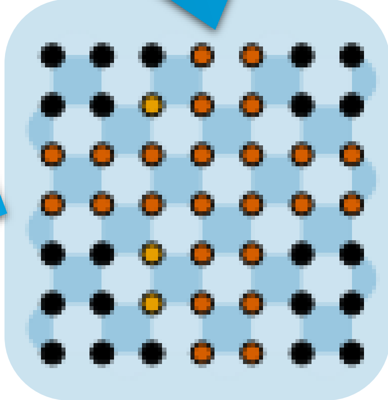
to leading order in p_{phys} under code-capacity level noise p_{phys}.

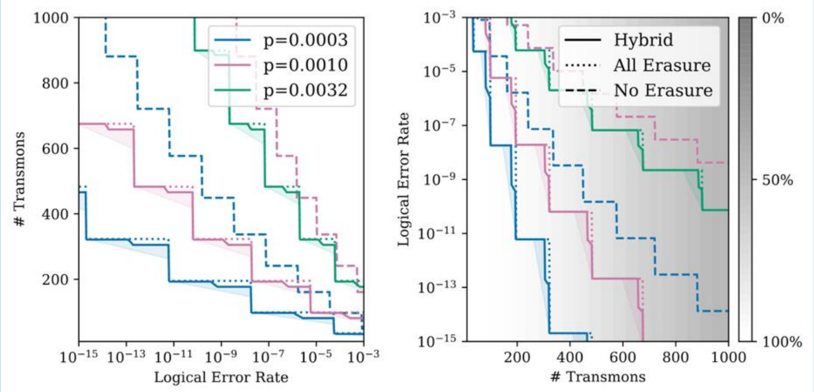
Circuit Level Simulations



Cost Comparisons

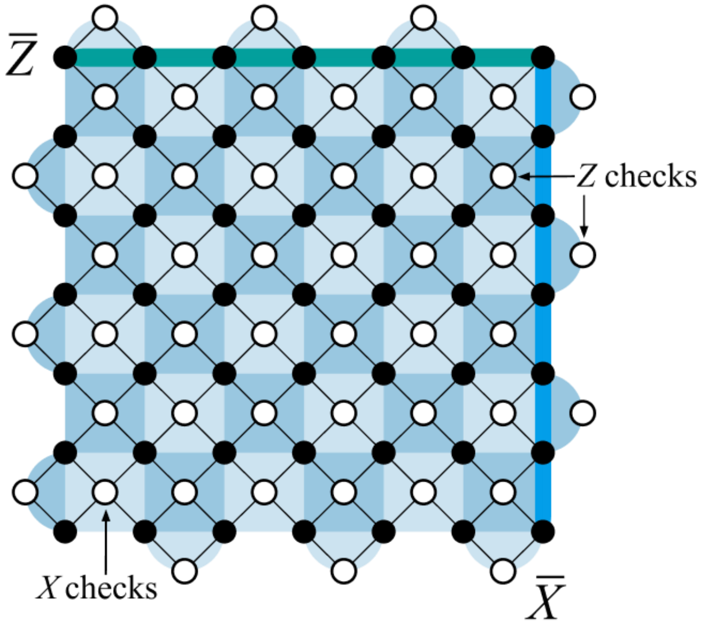
Optimized Placements



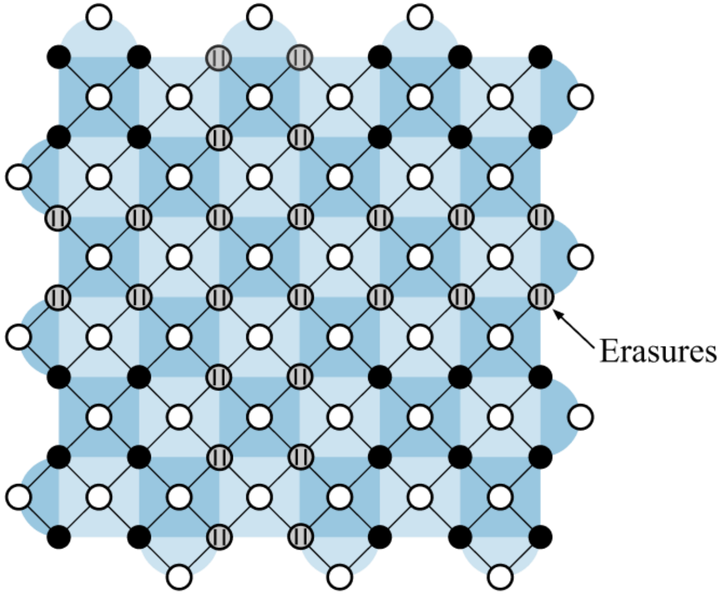


Understanding Partial Erasures

The Hybrid Erasure Surface Codes



Surface Code
$d = 7$



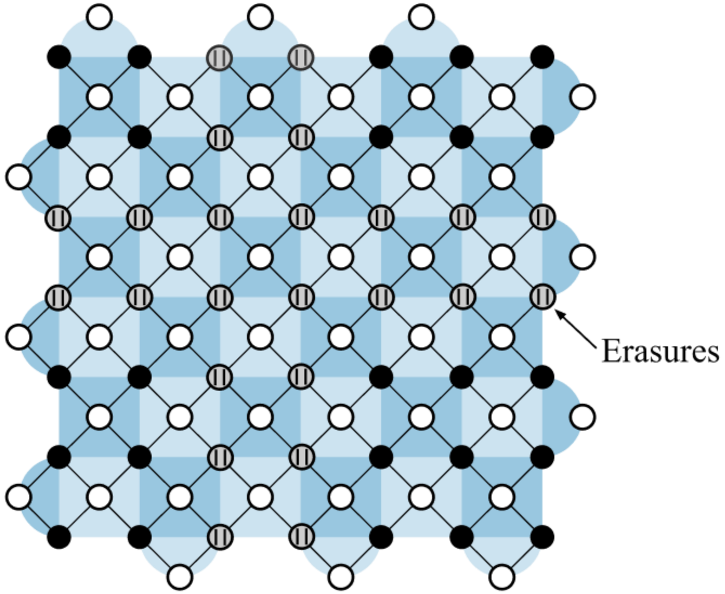
Hybrid Erasure
$(d, f_e, P) = (7, 50\%, P^*)$

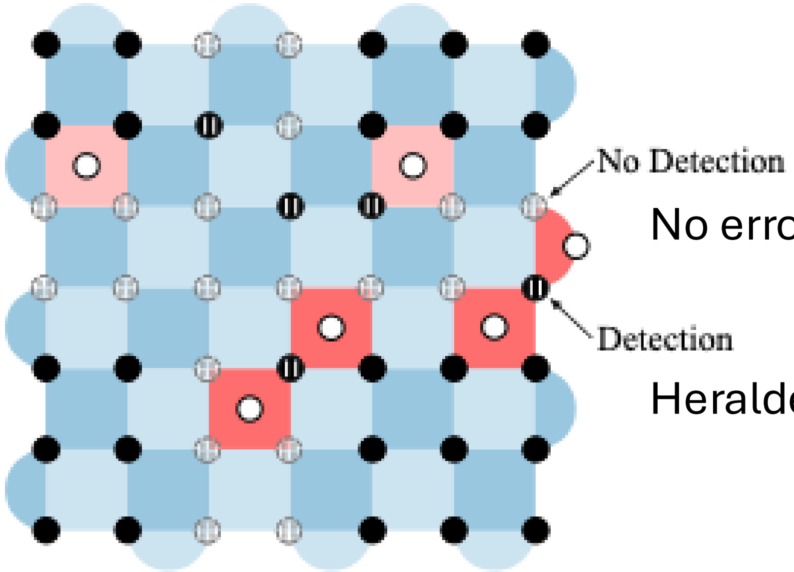
d: Distance

f_e: Erasure Fraction

P: Placements

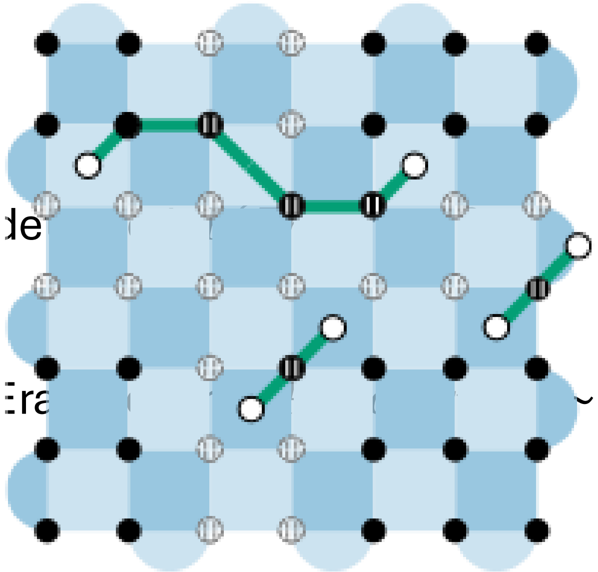
The Hybrid Erasure Surface Codes





No errors de

Heralded Era ~ 25%



Hybrid Erasure

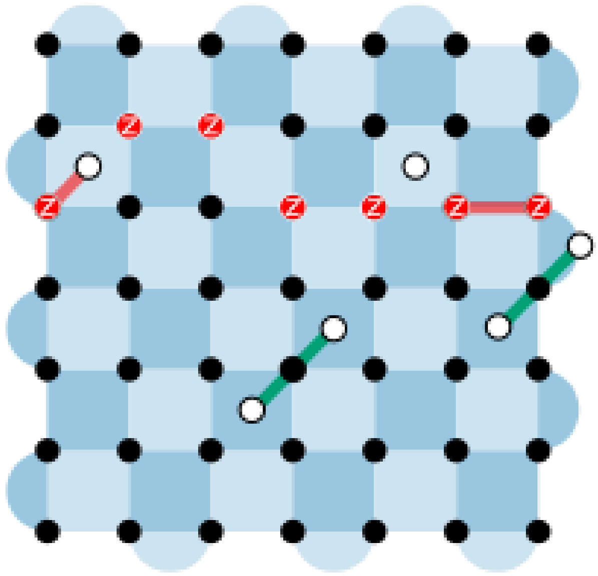
$(d, f_e, P) = (7, 50\%, P^*)$

Erasure Check

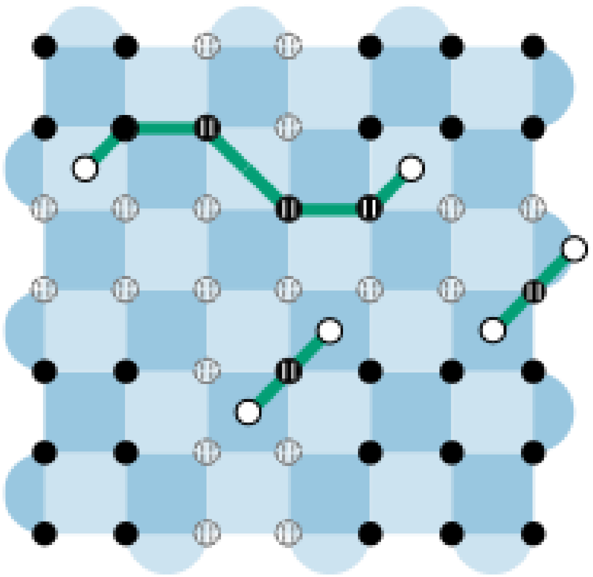
Before Syndrome Extraction

Decoding with updated priors

The Hybrid Erasure Surface Codes



Surface Code
$d = 7$
$d_{eff} = \lfloor \frac{d+1}{2} \rfloor = 4$



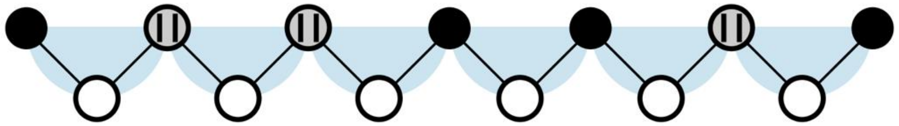
Hybrid Erasure
$(d, f_e, P) = (7, 50\%, P^*)$
$d_{eff} = ?$

Chain of physical errors
→ Logical errors

$$p \rightarrow \left(\frac{p}{p_{th}}\right)^{d_{eff}}$$

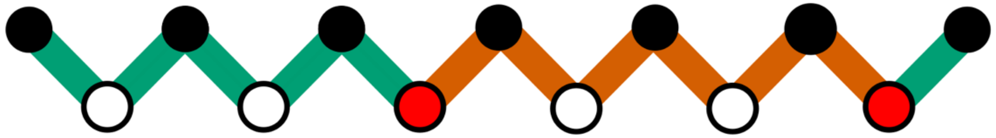
d_{eff}: Effective Distance
p_{th}: Threshold

Toy model: Repetition Code

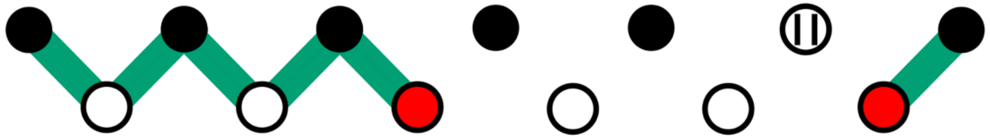


d: Number of data qubits
k: Number of erasure qubits

- Only two possible explanations

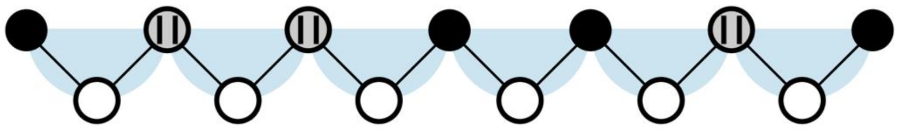


- Logical error only when all erasure qubits are triggered!

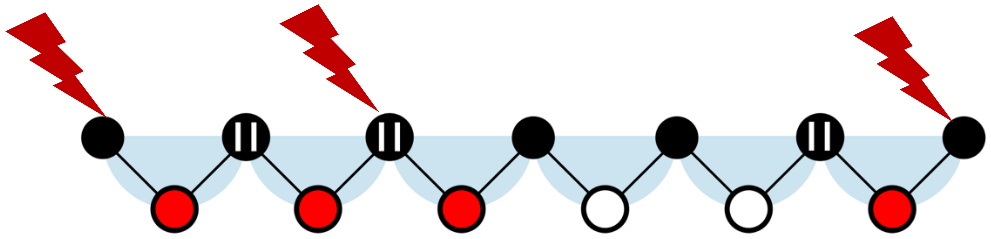


Placements doesn't matter!

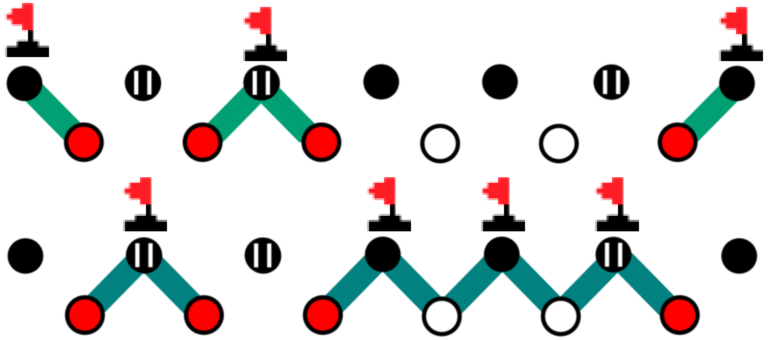
Toy model: Repetition Code



d: Number of data qubits
k: Number of erasure qubits



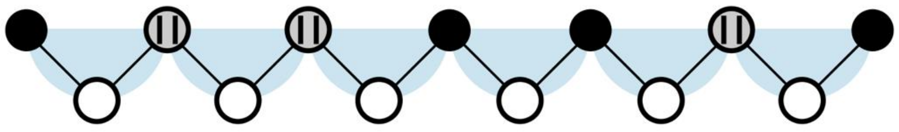
l_e: Number of erasure qubit errors
l_d: Number of standard data qubit errors



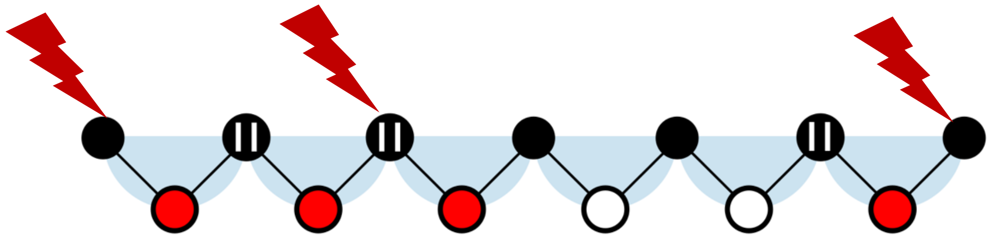
$$\mathbb{P}[E_1] = p^{l_d} \times (1-p)^{d-k-l_d} \times \frac{1}{2^{l_e}} \times \frac{1}{2^{k-l_e}}$$

$$\mathbb{P}[E_2] = p^{d-k-l_d} \times (1-p)^{l_d} \times \frac{1}{2^{k-l_e}} \times \frac{1}{2^{l_e}}$$

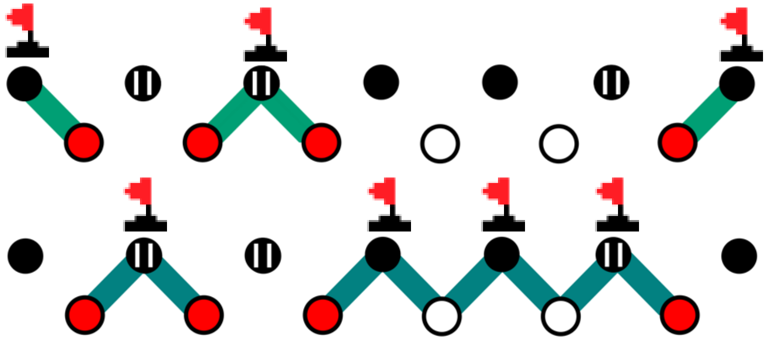
Toy model: Repetition Code



d: Number of data qubits
k: Number of erasure qubits



l_e: Number of erasure qubit errors
l_d: Number of standard data qubit errors

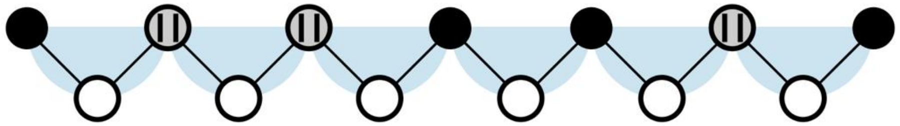


Logical error happens when:

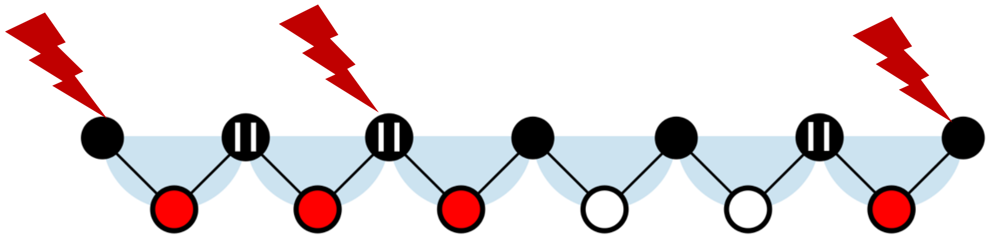
$$\mathbb{P}[E_1] < \mathbb{P}[E_2]$$

$$d_{eff}\ l_d \geq \left\lfloor \frac{d+k+1}{2} \right\rfloor$$

Toy model: Repetition Code



d: Number of data qubits
k: Number of erasure qubits

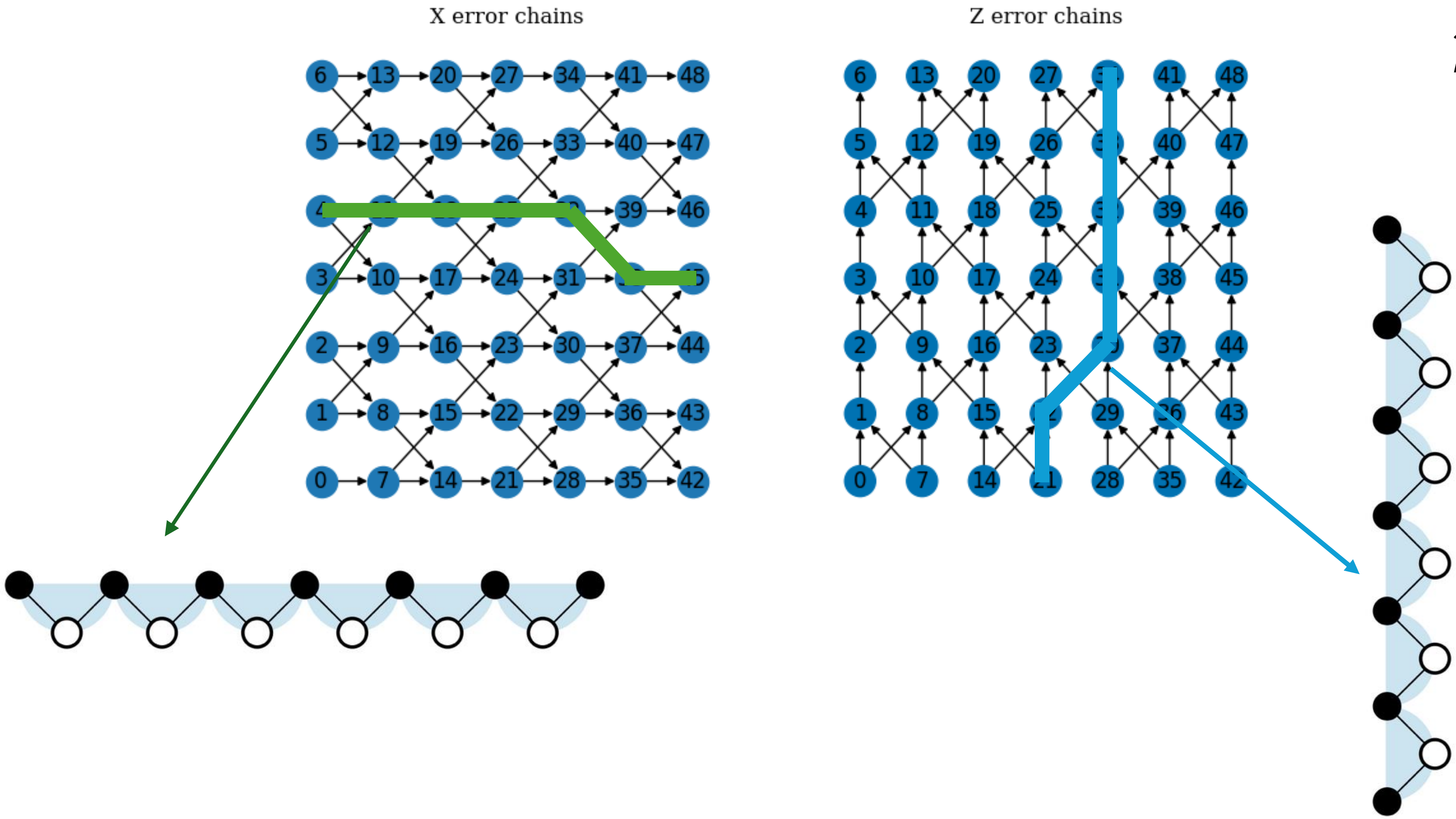


l_e: Number of erasure qubit errors
l_d: Number of standard data qubit errors

$$d_{eff} = \left\lfloor \frac{d + k + 1}{2} \right\rfloor$$

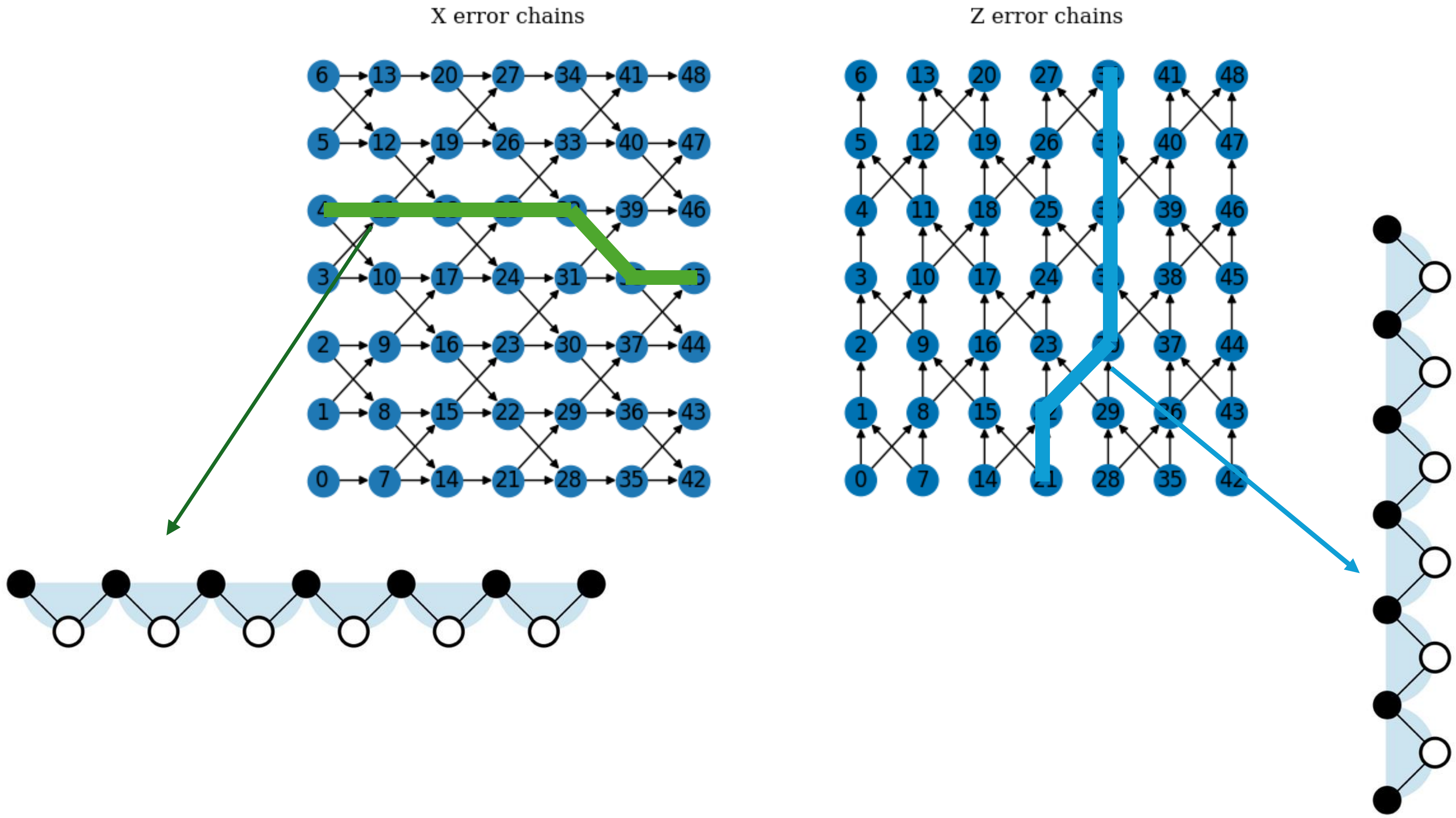
* For every two erasures added, effective distance increases by 1

Generalizing to surface codes



$$p_L \sim \mathbb{E}_{Paths}\,[\mathbb{P}[Error|Path]]$$

Generalizing to surface codes

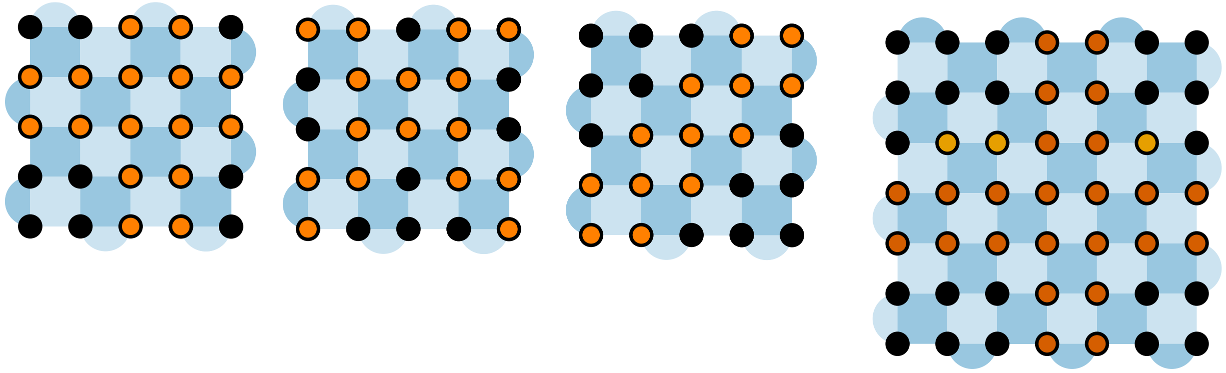


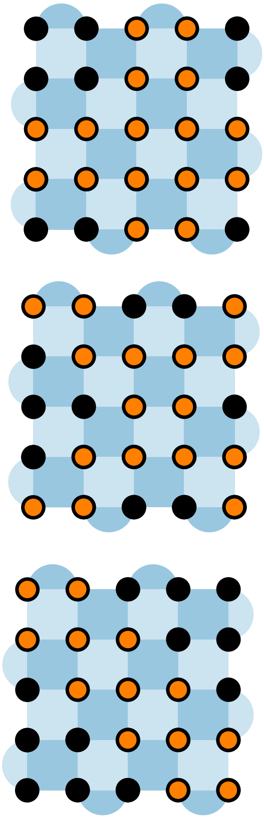
\# erasures in path P

$$p_L \sim \frac{1}{N} \sum_{P:Paths} p^{\left\lfloor \frac{d+k_P+1}{2} \right\rfloor}$$

Min # erasures in any paths

$$p_L \lesssim p_{phys}^{\lfloor (d+k+1)/2 \rfloor}$$





erasures in path P

$$p_L \sim \frac{1}{N} \sum_{P:Paths} p^{\left\lfloor \frac{d+k_P+1}{2} \right\rfloor}$$

Min # erasures in any paths

$$p_L \lesssim p_{phys}^{\lfloor (d+k+1)/2 \rfloor}$$

Optimal Placements

Heuristics #1: Impermeable walls

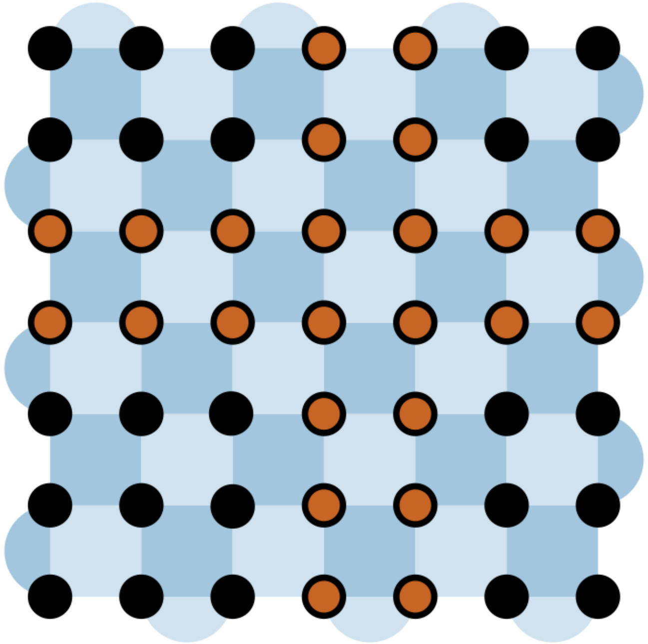
erasures in path P

Min # erasures in any paths

$$p_L \sim \frac{1}{N} \sum_{P:Paths} p^{\left\lfloor \frac{d+k_P+1}{2} \right\rfloor}$$

$$p_L \lesssim p_{phys}^{\lfloor (d+k+1)/2 \rfloor}$$

- Fill rows & columns to maximize k

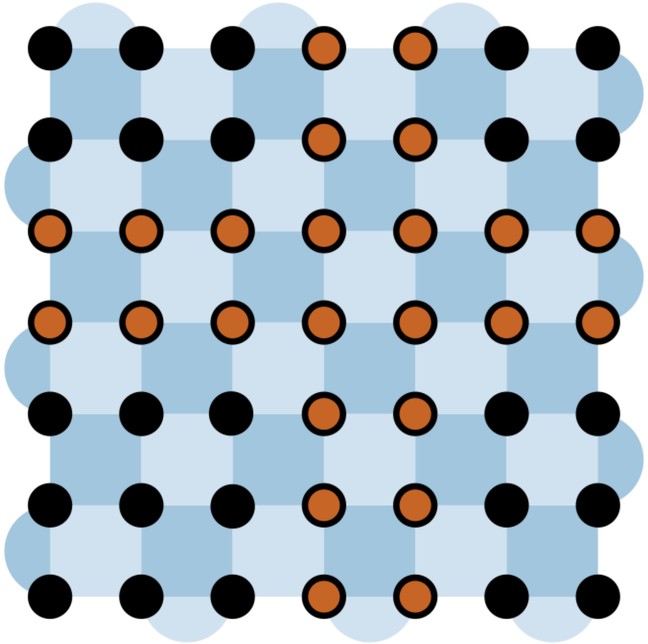


Heuristics #1: Impermeable walls

\# erasures in path P

Min # erasures in any paths

$$p_L \sim \frac{1}{N} \sum_{P:Paths} p^{\left\lfloor \frac{d+k_P+1}{2} \right\rfloor} \qquad p_L \lesssim p_{phys}^{\lfloor (d+k+1)/2 \rfloor}$$



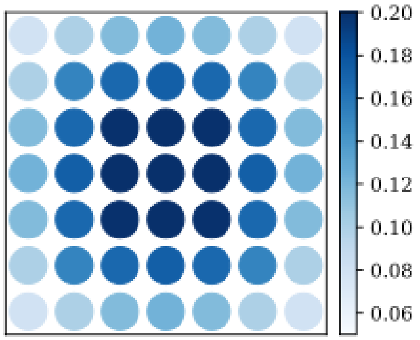
- Fill rows & columns to maximize k
- $d_{eff} \geq \left\lfloor \frac{d\times\left(2-\sqrt{1-f_e}+1\right)}{2} \right\rfloor - \epsilon$

Heuristics #2: Voracious Core

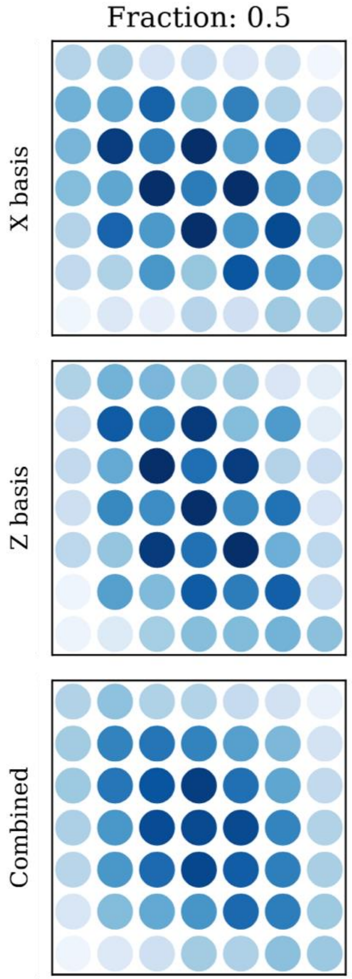
 # *erasures in path P* Min # erasures in any paths

$$p_L \sim \frac{1}{N} \sum_{P:Paths} p^{\left\lfloor \frac{d+k_P+1}{2} \right\rfloor} \qquad p_L \lesssim p_{phys}^{\lfloor (d+k+1)/2 \rfloor}$$

- Maximize the number of paths that contains the placed erasure



Analytical Path Counting



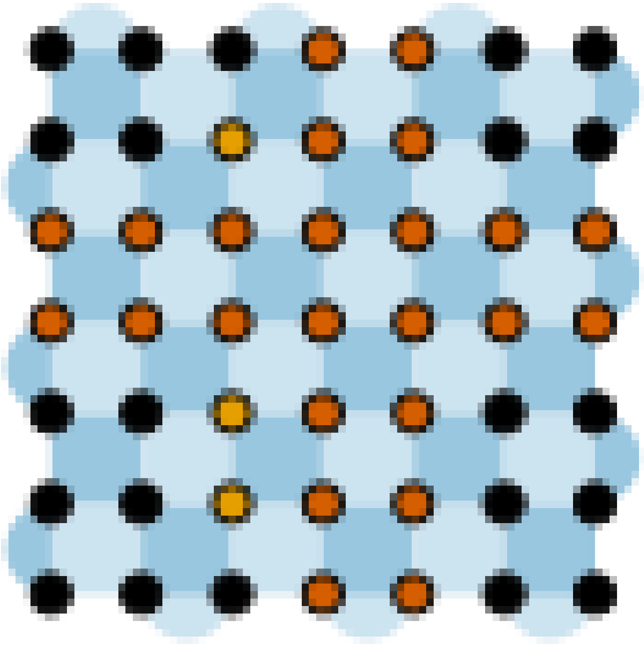
Simulations

Heuristics #2: Voracious Core

 # erasures in path P Min # erasures in any paths

$$p_L \sim \frac{1}{N} \sum_{P:Paths} p^{\left\lfloor \frac{d+k_P+1}{2} \right\rfloor} \qquad p_L \lesssim p_{phys}^{\lfloor (d+k+1)/2 \rfloor}$$

- Maximize the number of paths that contains the placed erasure
- Closest to center



Optimized Placements

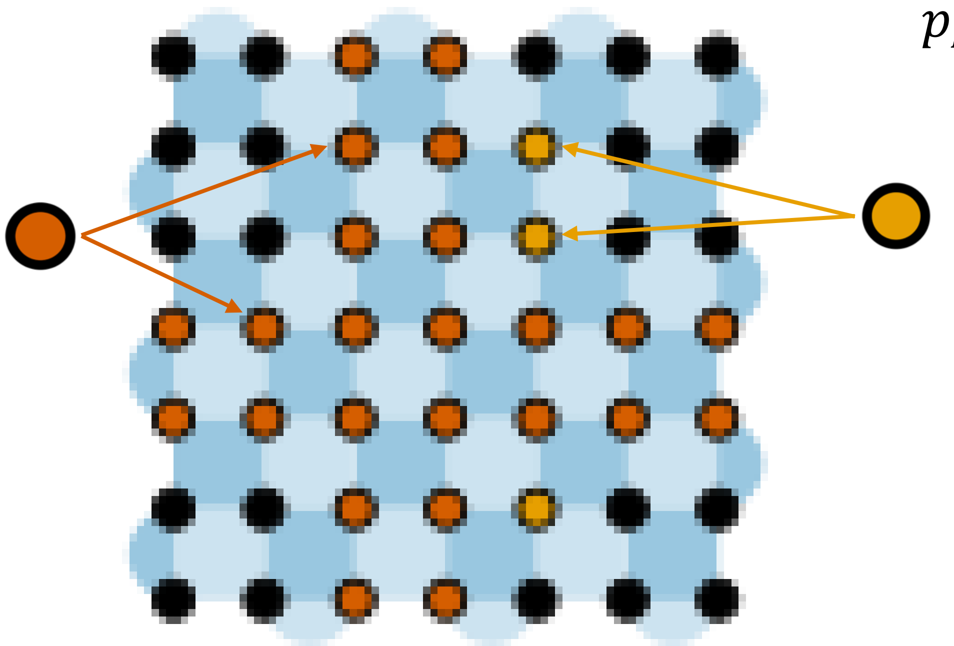
Min # erasures in any paths

$$p_L \lesssim p_{phys}^{\lfloor (d+k+1)/2 \rfloor}$$

erasures in path P

$$p_L \sim \frac{1}{N} \sum_{P:Paths} p^{\left\lfloor \frac{d+k_P+1}{2} \right\rfloor}$$

1. Prioritize filling rows/columns

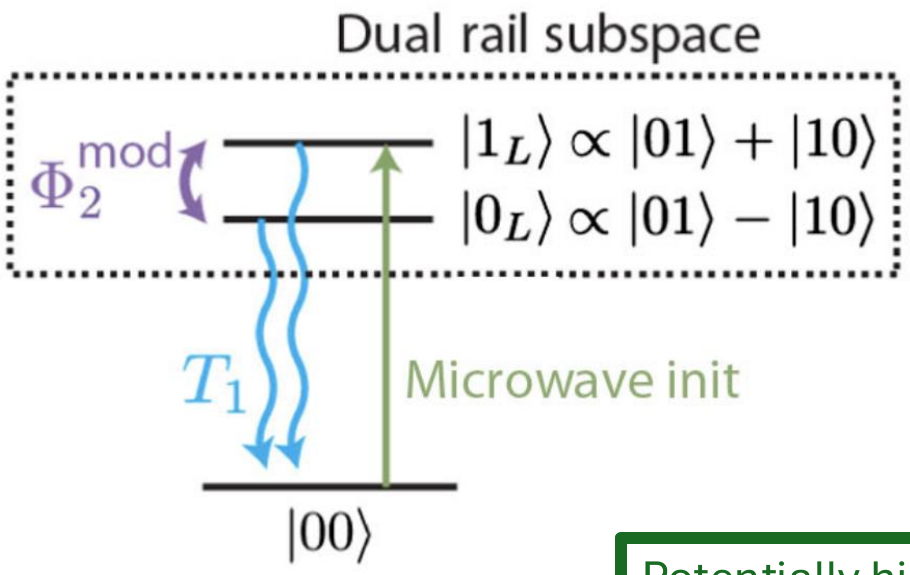


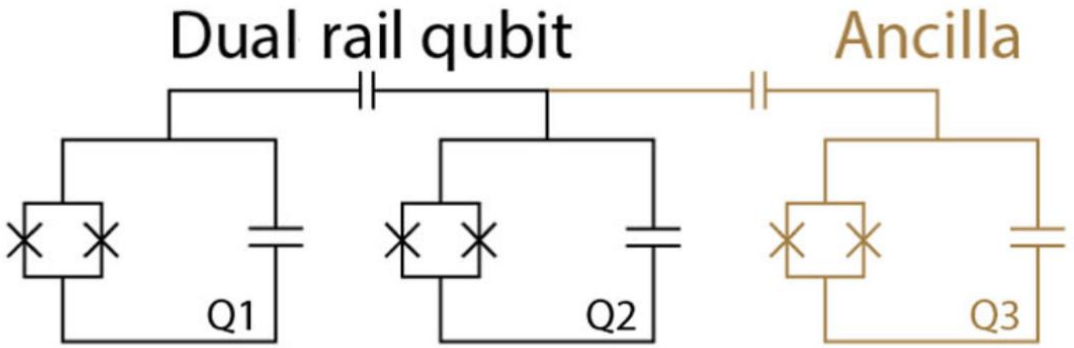
2. Place the rest closest to center

Part 2: Simulations and results

Jason Chadwick

Applying to dual-rail transmons

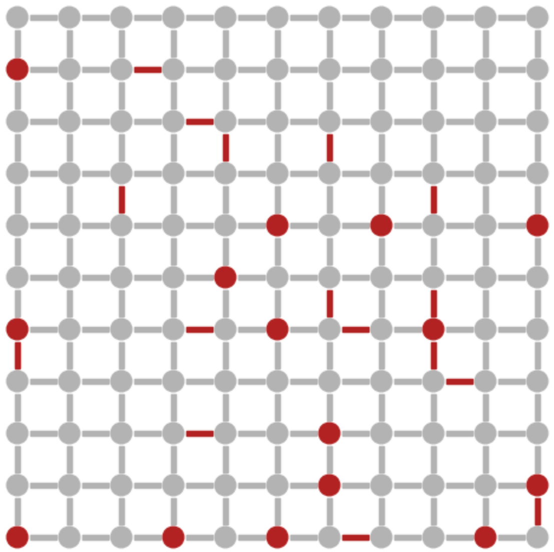




Potentially higher error rate, but errors are strongly biased towards erasures

Levine et al., “Demonstrating a Long-Coherence Dual-Rail Erasure Qubit Using Tunable Transmons”, PRX 14, 011051 (2024)

Why do we care about transmon count?



Wiring complexity

Yield constraints

Cooling capacity

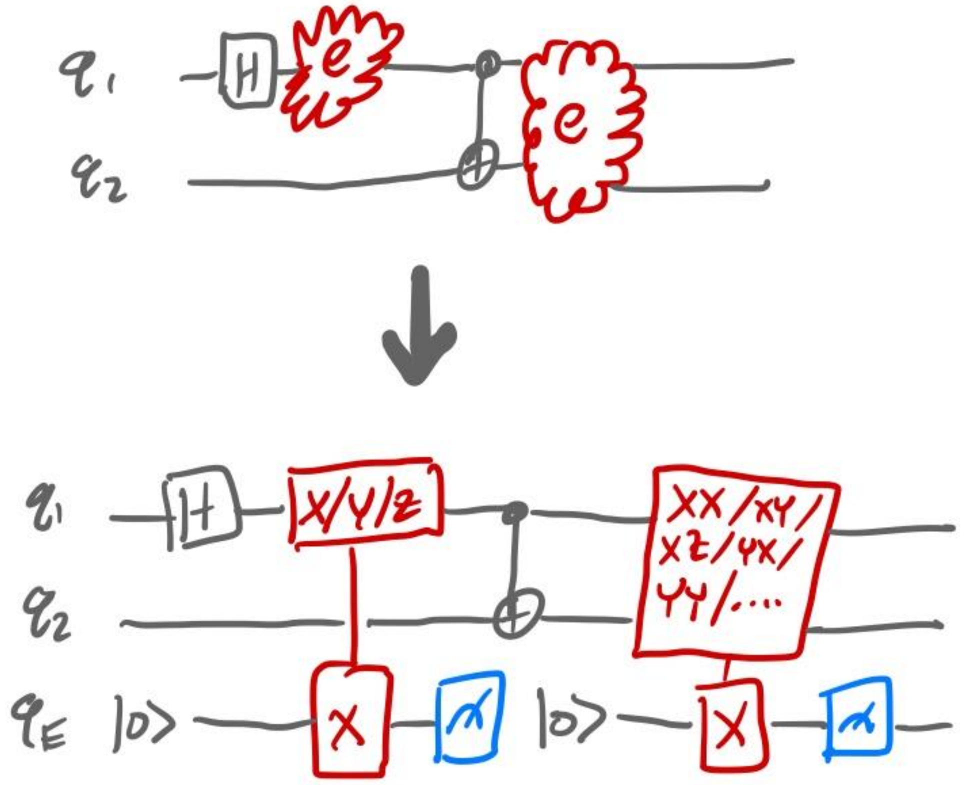
System cost

Noise model

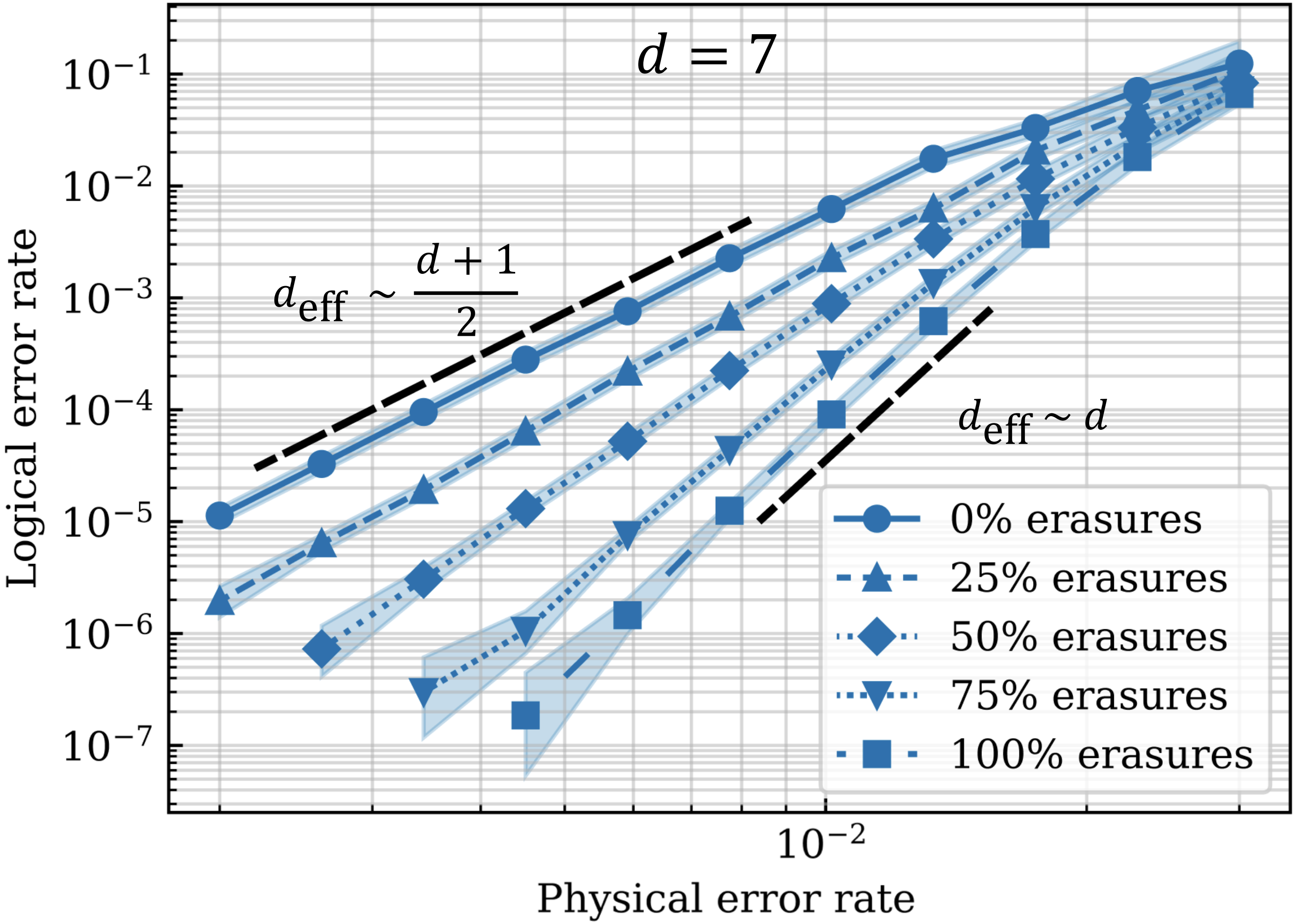
Error mechanism	Standard qubit	Dual-rail erasure qubit
Initialization error	p	$2p$
Readout error	p	$2p$
Single-qubit (H) gate error	$p/10$	p
Two-qubit (CX) gate error	p	p
Erasure check error	-	p

Simulating erasures in Stim

- Stim: fast simulator for QEC, only supports Cliffords
- One "erasure flag" qubit q_E initialized in $|0\rangle$
- Erasure error depolarizes qubits and applies X on q_E
- DETECTOR on erasure flag result informs decoder of erasure information

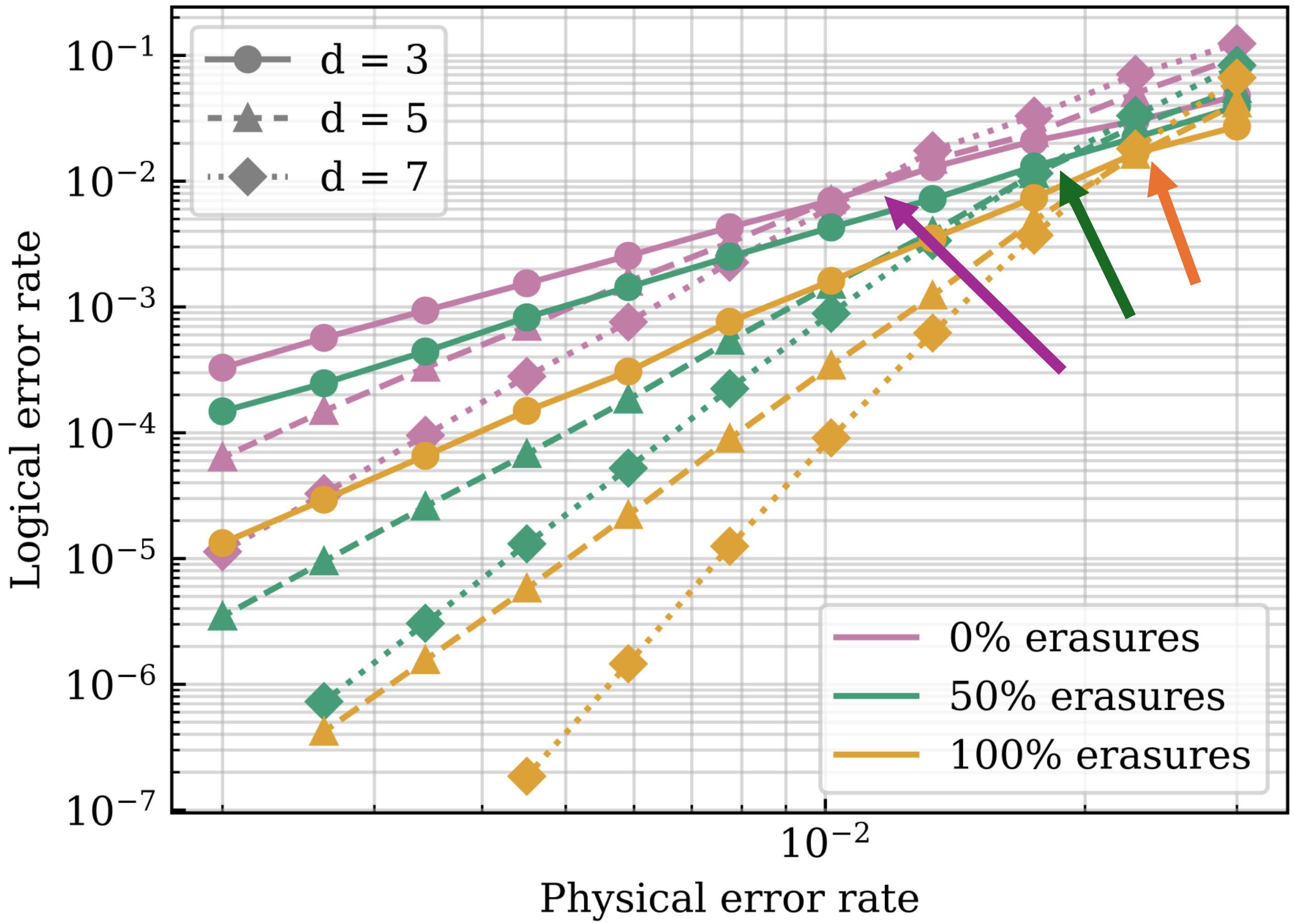


Effective distance



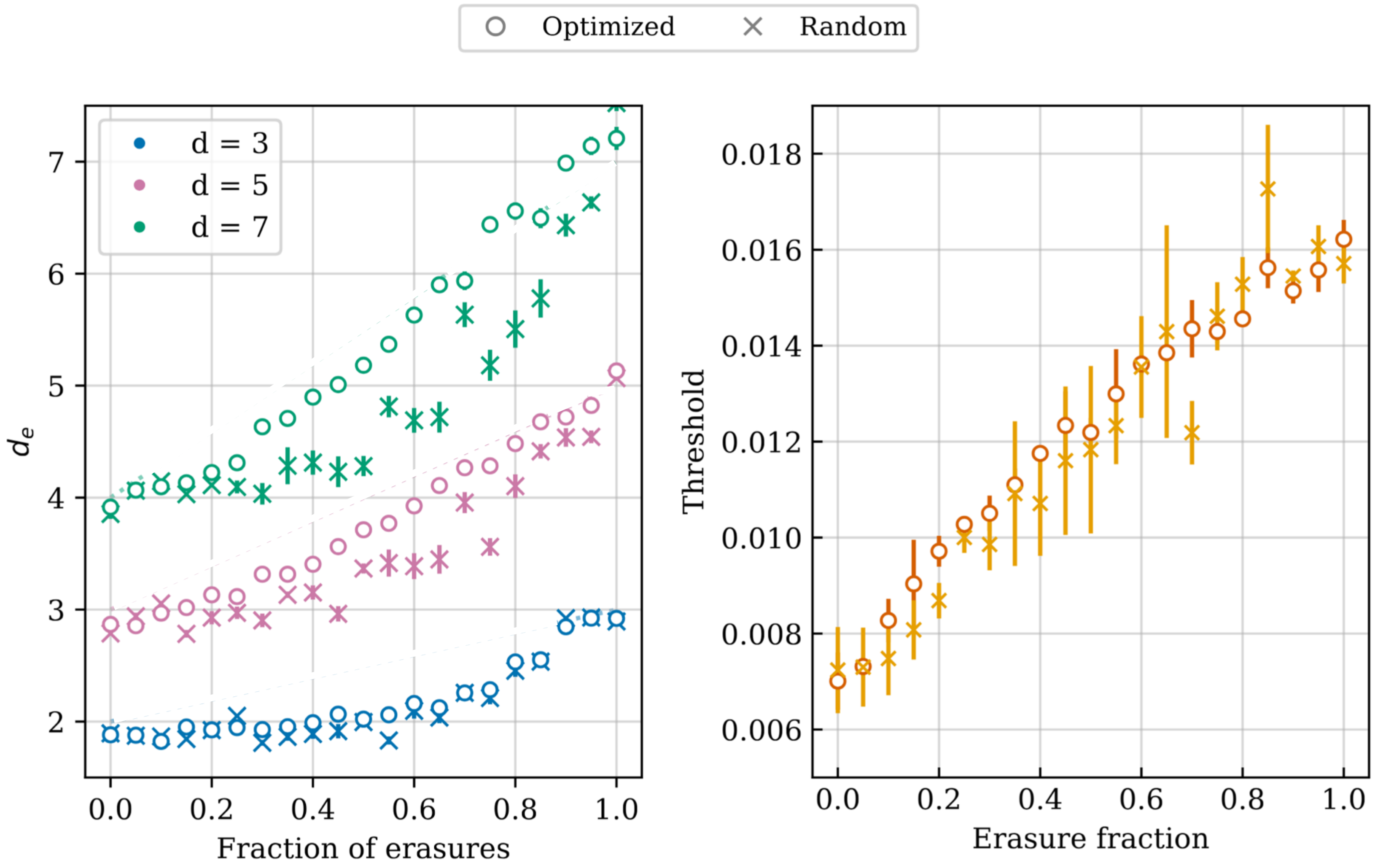
$$p \rightarrow \left(\frac{p}{p_{th}}\right)^{d_{eff}}$$

Threshold



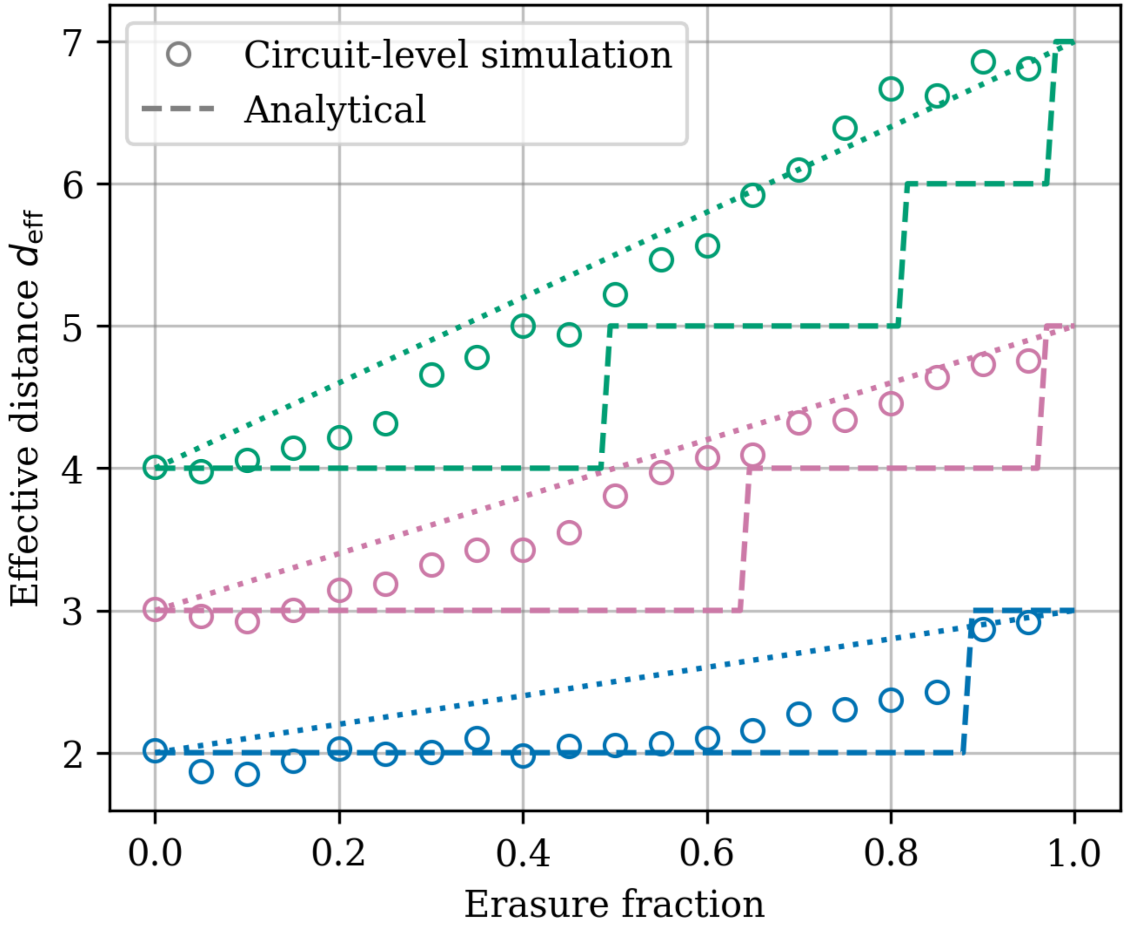
$$p \rightarrow \left(\frac{p}{p_{th}}\right)^{d_{eff}}$$

Trends

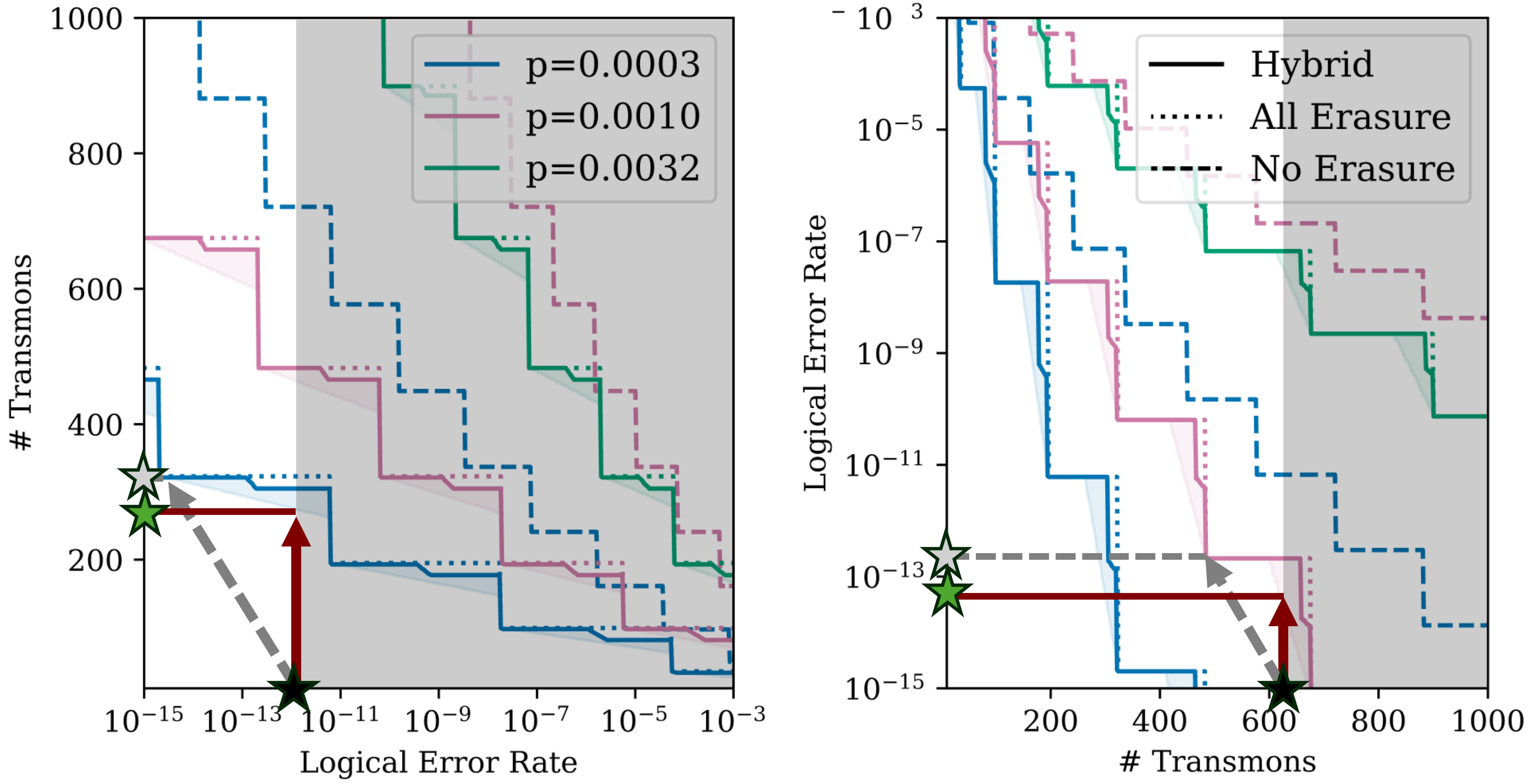


Optimized
Random
d = 3
d = 5
d = 7
d_e
Fraction of erasures
Threshold
Erasure fraction

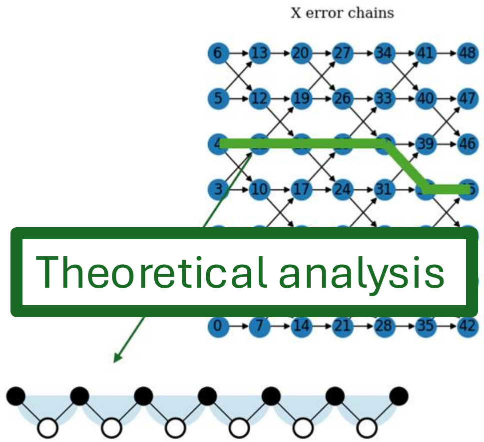
Comparing to code-capacity model



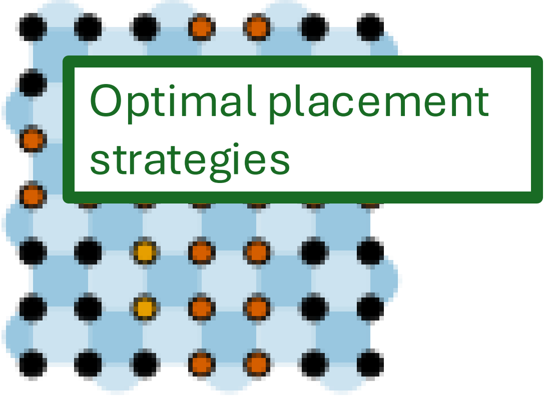
Scaling costs



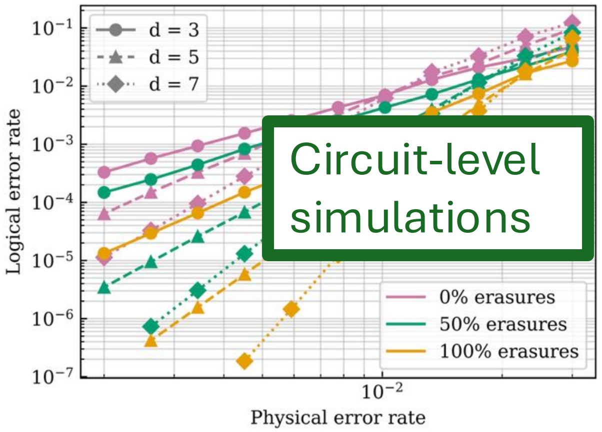
Summary



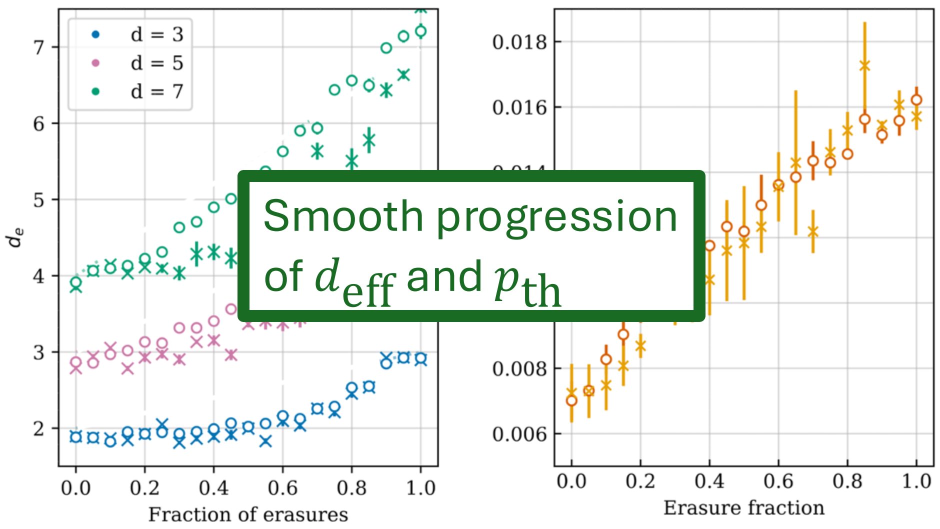
Theoretical analysis



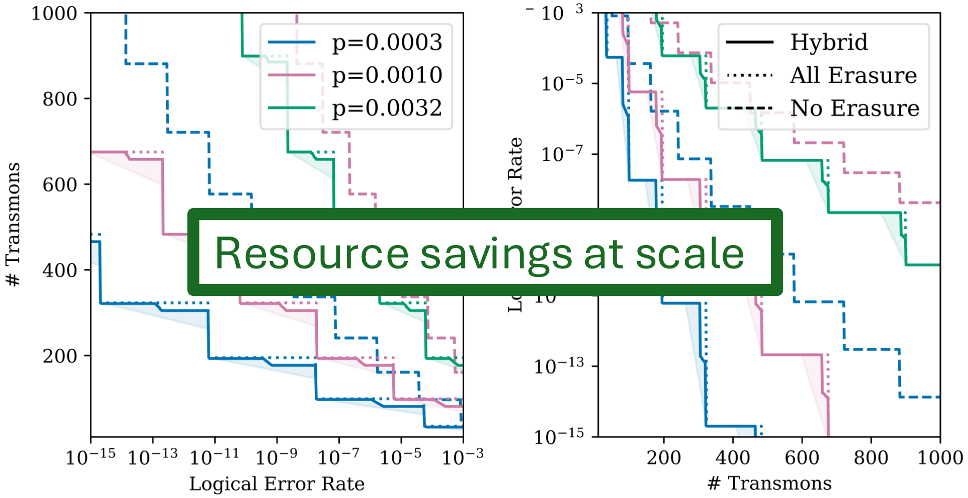
Optimal placement strategies



Circuit-level simulations



Smooth progression of d_{eff} and p_{th}



Resource savings at scale

Jason Chadwick

STIM + Circuit Level Simulation

Mariesa Teo

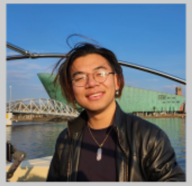
Numerical Experiments

Joshua Viszlai

STIM + Cost Analysis

Willers Yang

Theoretical Analysis



Fred Chong

Principal Investigator

THE UNIVERSITY OF CHICAGO

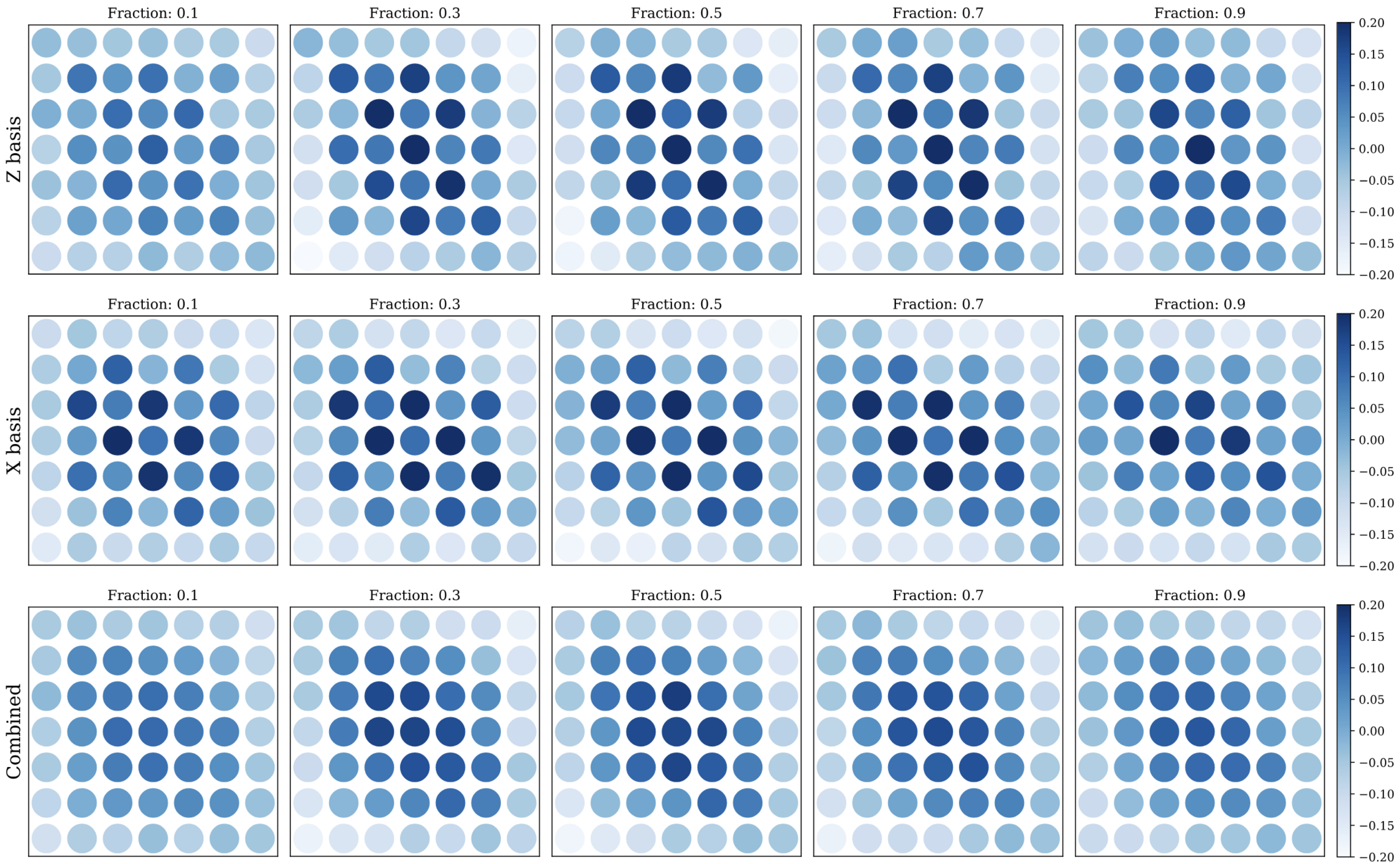
Thank you for your attention!

jchadwick@uchicago.edu

willers@uchicago.edu

arXiv:2505.00066

Bonus slides


Fraction: 0.1
Fraction: 0.3
Fraction: 0.5
Fraction: 0.7
Fraction: 0.9
Z basis
X basis
Combined
0.20
0.15
0.10
0.05
0.00
−0.05
−0.10
−0.15
−0.20